REMARKS

Claims 1, 3-17, 19-44, 46-47, and 49-122 are currently pending in this application. In the Office Action dated September 22, 2006, the Examiner took the following action: (1) rejected claims 15, 33, 64, 71, 76, 80, 82-83, 90, 96, 101 and 104 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement; (2) objected to claims 49-52 as being dependent upon canceled claim 48; (3) rejected claims 1, 3-14, 17, 19-32, 34, 36, 38-44, 47, 49-63, 66-70, 73-75, 78-79, 84-89, 91, 93-95, 97, 99-100, 102, 105, 107 and 118-121 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,443,845 to Hamilton et al. ("Hamilton") and further in view of U.S. Patent No. 6,301,637 to Krull et al. ("Krull"); and (4) rejected claims 16, 35, 37, 46, 57, 65, 72, 77, 81, 92, 98, 103, 106, 108-117 and 122 under 35 U.S.C. § 103(a) as being unpatentable over Hamilton and Krull as applied to claims 1, 17 and 47 above, and further in view of U.S. Patent No. 6,434,654 to Story et al.

Rejections under 35 U.S.C. §112 ¶1

Claims 15, 33, 64, 71, 76, 80, 82-83, 90, 96, 101 and 104 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicant respectfully asserts that the written description requirement has been satisfied with respect to the claim term "coupling a packet of data." The application as filed discusses coupling of packets between components of the memory system and Applicant respectfully asserts that the use of the term "coupling" to refer to the transfer of data on a bus is clear to those skilled in the art of data transfer over a bus system. However, notwithstanding the adequacy of the original claim language, the claims have been amended to recite "transmitting" packets of data, in order to expedite prosecution of the present application.

Objections to the Claims

Claims 49-52 are objected to as being dependent upon canceled claim 48. By this amendment claims 49-52 have been amended to depend from claim 47.

Discussion of the Disclosed Embodiment

The disclosed embodiments of the invention will now be discussed in comparison to the prior art. Of course, the discussion of the disclosed embodiments, and the discussion of the differences between the disclosed embodiments and the prior art subject matter, do not define

the scope or interpretation of any of the claims. Instead, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

In one disclosed embodiment, a memory system includes a memory hub controller coupled to at least one memory module having a memory hub and a number of memory devices coupled to the memory hub. The memory hub is coupled to the memory hub controller by a bus having a fixed number of lines. Command, address and data signals are coupled from the memory hub controller to the memory hub over the bus. Some of the lines of the bus are used for carrying data to the memory hub while the remaining wires carry data to the memory hub controller. During operation of the memory system, the volume of data flowing to and from the memory hub is monitored. The number of lines carrying data to the memory hub may be reduced or increased according to which direction has a higher volume of traffic, with the remaining lines being used to carry data to the memory hub controller such that the total number of lines remains fixed. Adjustments to the number of lines may also be based on anticipated volumes of data traffic.

The novel system discosed provides the important benefit that bottlenecks between the memory hub and memory hub controller are reduced by adapting the capacity according to current needs.

Discussion of the Cited References

Hamilton discloses a modular input/output system for a calculator. The device of Hamilton includes a number of buffers each having an address decode coupling the buffers to buses. Fig. 12A. The buffers are also coupled to bonding pads for transferring data to and from the buffers. The address decode is programmable such that the function of the buffer may be changed to adapt the I/O system for use with a particular architecture. Col. 12, 8-11 ("Each buffer has its own associated address decode which individually decodes its own predefined select address, and is selectively either written into or read from.")

Hamilton differs substantially from the disclosed embodiment in that the number of communication lines dedicated to input and output to a buffer does not change. Hamilton only discloses an address bus, a data bus, a power bus, and a display voltage bus statically coupled to a buffer. Col. 12, lns. 3-8 ("...each buffer is provided with its own associated memory address decode 225-228. This allows a common address bus 212, data bus 213, control and clock lines

311 and power buses 214 and 215, to be coupled in parallel to each of the I/O buffer locations."). Hamilton does not teach changing the number of bus lines carrying data to the buffer or otherwise altering the function of the buses is alterable in any way. Hamilton further does not alter the use of the bus lines in accordance to a volume of data traffic. The number of inbound and outbound bus lines in Hamilton is not varied such that the total number of input and output lines is fixed.

Story discloses a "system bus with a variable width selectively configurable at initialization." The system includes a bridge that provides an interface between a host PCI and a companion PCI. To accommodate differences in the widths of the buses on the host and companion PCI, an initialization protocol is used to establish the effective width during initialization of the data bus." Col. 8, lns. 25-29. The bus width may be varied between "1, 4, 8, and 16 bits." Col. 8, lns. 21-22.

Story only discloses varying the bus width between 1, 4, 8, and 16 bits, which means the number of bus lines used is not fixed. Story does not change the number of upstream and downstream lines such that the sum of upstream and downstream lines is fixed. Story teaches only that the bus width is changed to accommodate the capacity of the companion device, not according to the amount of traffic on the bus. Story further simply changes the width of the bus, not the direction of data flow on particular bus lines.

Krull fails to remedy the deficiencies of Hamilton and Story.

Discussion of the Claims

Turning now to the claims, none of the cited references teach, in combination with the other limitations of claim 1, a method including the step of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity; coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity, *where the sum of the first capacity and the second capacity is a fixed value; and altering the first capacity and the second capacity during the operation of the memory system based on the rate at which the signals are being coupled from the memory hub controller to the memory hub in the at least one memory module and based*

on the rate at which the signals are being coupled from the memory hub in the at least one memory module to the module memory hub controller." (emphasis added)

Claims 3-16 are dependent on claim 1 and are therefore allowable

With respect to claim 17, none of the cited references teach, in combination with the other limitations of the claim, the steps of "coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M; and altering the values of N and P during the operation of the memory system based on the rate at which signals are being coupled through the bus."

Claims 19-35 are dependent on allowable claim 17 and are therefore allowable.

With respect to claim 36, none of the cited references teach, in combination with the other limitations of the claim, a memory system having "a memory hub controller having M buffers, N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, *the values of N and P being alterable during the operation of the memory system*; ... and a bus having M signal lines each of which is coupled between a respective buffer of the memory hub controller and a respective buffer of the memory hub, *the value of M being equal to the sum of N and P and the values of N and P further being altered within a range of minimum and maximum values of N and P respectively.*" (emphasis added).

Claims 37-44 and 46 are dependent on allowable claim 36 and are therefore allowable.

With respect to claim 47, none of the cited references teach, in combination with the other limitations of the claim, a processor-based system having "a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus having a width of M bits, *the value of M being variable to adjust that bandwidth of the downstream bus and the value of M further being alterable based on the rate at which the signals are being coupled through*; and an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, *the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth of the upstream bus and the value of N further being alterable based on the rate at which the signals are being coupled through.*" (emphasis added).

Claims 49-57 are dependendent on allowable claim 47 and are therefore allowable.

With respect to claim 58, none of the cited references teach in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; altering the first capacity and the second capacity during the operation of the memory system.*" (emphasis added).

Claims 59-65 depend on allowable claim 58 and are therefore allowable.

With respect to claim 66, none of the cited references teach, in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; and altering the first capacity and the second capacity during the operation of the memory system based on the rate at which it is anticipated that the signals will be coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which it is anticipated that the signals will be coupled from the memory hub in the at least one memory module to the module memory hub controller.*" (emphasis added).

Claims 67-72 depend on allowable claim 66 and are therefore allowable.

With respect to claim 73, none of the cited references recite, in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a*

communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; and altering the first capacity and the second capacity during the operation of the memory system within a range of minimum and maximum values for the first capacity and the second capacity respectively." (emphasis added).

Claims 74-77 depend on allowable claim 73 and are therefore allowable.

With respect to claim 78, none of the cited references teach in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; and manually altering the first capacity and the second capacity during the operation of the memory system.*"'

Claims 79-81 depend on allowable claim 78 and are therefore allowable.

With respect to claim 82, none of the cited references teach, in combination with the other limitations of the claim, a method including the steps of "coupling signals in a packet that includes command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using a communications path having a first capacity*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using a communications path having a second capacity, where the sum of the first capacity and the second capacity is a fixed value; and altering the first capacity and the second capacity during the operation of the memory system.*" (emphasis added).

Claim 83 depends on allowable claim 82 and is therefore allowable.

With respect to claim 84, none of the cited references teach in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using N of the M signal lines of the bus*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using P of the M signal lines of the bus, where N+P = M; and altering the values of N and P during the operation of the memory*

system by configuring buffers in the memory hub controller and in the memory hub of the at least one memory module as either input buffers or output buffers." (emphasis added).

Claims 85-92 depend on allowable claim 84 and are therefore allowable.

With respect to claim 93, none of the cited references teach, in combination with the other limitations of the claim a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using N of the M signal lines of the bus*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using P of the M signal lines of the bus, where N+P = M; and altering the values of N and P during the operation of the memory system, the values of N and P being within a range of minimum and maximum values of N and P respectively.*" (emphasis added).

Claims 94-98 depend on allowable claim 93 and are therefore allowable.

With respect to claim 99, none of the cited references teach, in combination with the other limitations of claim 99, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using N of the M signal lines of the bus; coupling data signals from the memory hub in the at least one memory module to the memory hub controller using P of the M signal lines of the bus, where N+P = M; and manually altering the values of N and P during the operation of the memory system."

Claims 100-103 depend on allowable claim 99 and are therefore allowable.

With respect to claim 104, none of the cited references teach, in combination with the other limitations of the claim, a method including the steps of "coupling signals in a packet that includes command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using N of the M signal lines of the bus*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using P of the M signal lines of the bus, where N+P = M; and altering the values of N and P during the operation of the memory system.*" (emphasis added).

Claims 105-106 are dependent on allowable claim 104 and are therefore allowable.

With respect to claim 107, none of the cited references teach, in combination with the other limitations of the claim, a method including the steps of "coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module *using N of the M signal lines of the bus and further using a uni-directional downstream bus having N signal lines*; coupling data signals from the memory hub in the at least one memory module to the memory hub controller *using P of the M signal lines of the bus and further using a uni-directional upstream bus having P signal lines, where N+P = M; and altering the values of N and P during the operation of the memory system.*" (emphasis added).

Claim 108 is dependent on allowable claim 107 and is therefore allowable.

With respect to claim 109, none of the cited references teach, in combination with the other limitations of the claim, a memory system including "a memory hub controller having M buffers, *N of the M buffers being configured as output buffers and P of the M buffers being configured as input buffers, the values of N and P being alterable during initialization of the memory system*...[and] a bus having M signal lines each of which is coupled between a respective buffer of the memory hub controller and a respective buffer of the memory hub, *the value of M being equal to the sum of N and P.*" (emphasis added).

Claims 110-117 depend on allowable claim 109 and are therefore allowable.

With respect to claim 118, none of the cited references teach, in combination with the other limitations of the claim, a processor-based system including "a downstream bus coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus having a width of M bits, *the value of M being variable to adjust that bandwidth of the downstream bus and the value of M further being alterable based on the rate at which it is anticipated that the signals will be coupled through at least the downstream bus*; and an upstream bus coupled between the input port of the memory controller and the memory hub of the at least one memory module, *the upstream bus having a width of N bits where N is equal to a fixed value less M, the value of N being variable to adjust that bandwidth of the upstream bus and the value of N further being alterable based on the rate at which it is anticipated that the signals will be coupled through at least the upstream bus.*"

Claims 119-122 depend on allowable claim 118 and are therefore allowable.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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